Description

APPARATUS FOR GENERATING CLOCK PULSES USING A DIRECT DIGITAL SYNTHESIZER

Technical Field

[1] The present invention generally relates to an apparatus for generating clock pulses using a Direct Digital Synthesizer (DDS), and more particularly to an apparatus which produces a particular desired frequency by changing a Frequency Tuning Word (FTW) when generating the clock pulses using the DDS.

Background Art

[2] As is well known, in a CDMA2000 1X base station transmit system, a Digital Up-converter Card Assembly (DUCA) is used to generate 58.9824 MHz clock pulses. These pulses are used to perform all signal processing based on 19.6608 MHz reference clock pulses.

[3] As is shown in Fig. 1, a conventional clock generator using a Phase Locked Loop (PLL) is configured to generate 58.9824 MHz clock pulses in which their phase is locked with a 19.6608 MHz by PLL 10. PLL 10 comprises a phase detector 11, a low pass filter 12, and a Voltage Controlled Oscillator (VCO) 13.

[4] However, when the clock pulses are generated using a conventional clock generator with PLL 10 such as the one described above, the output clock frequency cannot vary in accordance with system performance. This is because the output clock frequency is fixed. Further, the quality of the output clock signal may become degraded due to jitter and phase noise.

Disclosure of Invention

Technical Problem

[5] As described above, the conventional clock generator using a PLL circuit is disadvantageous since the output clock frequency cannot be varied while the output clock signal may become degraded due to jitter and phase noise.

Technical Solution

[6] It is, therefore, an object of the present invention to provide an apparatus for generating clock pulses using a DDS having high frequency resolution. It should be noted that the frequency of the generated clock pulses is easily changeable and their signals are free from jitter and phase noise.

[7] In accordance with the present invention, there is provided an apparatus for

generating clock pulses using a DDS. Such apparatus comprises: (1) a DDS, which comprises a PLL multiplier for receiving system reference clock pulses of a first frequency, configured to convert the system reference clock pulses into a DDS operation clock signals of a second frequency; a phase accumulator for receiving a Frequency Tuning Word (FTW), accumulating a phase by the FTW, and outputting the phase of a particular desired frequency, wherein the phase accumulator operates using the DDS operation clock signals from the PLL multiplier; a phase-to-magnitude for, in responsive to the accumulated phase of the particular frequency from the phase accumulator, providing a clock signal having a magnitude corresponding to the phase of the particular frequency, wherein the phase-to-magnitude operates using the DDS operation clock signals from the PLL multiplier; a Digital-to-Analog (DA) converter for, in responsive to the clock signal from the phase-magnitude converter, converting the clock signal to an analog signal of a DDS output frequency, wherein the DA converter operates using the DDS operation clock signals from the PLL multiplier; (2) a band pass filter for bandpass-filtering the analog signal of the DDS output frequency from the DA converter to provide a bandpass-filtered signal; and (3) a comparator for, in responsive to the bandpass-filtered signal from the band pass filter, transforming the signal of the DDS output frequency into a square wave.

Advantageous Effects

[8] According to the present invention, a particular desired frequency may be produced by changing the FTW when generating the clock pulses using the DDS. This is so that the output frequency can be changed more flexibly than the conventional clock generator using a PLL. Further, better stable system clock pulses can be supplied by removing the jitter, phase noise, etc.

Brief Description of the Drawings

[9] The above and other objects and features in accordance with the present invention will become more apparent from the following description of a preferred embodiment given in conjunction with the accompanying drawings, in which:

[10] Fig. 1 is a functional block diagram of a conventional clock generator using a PLL.

[11] Fig. 2 is a functional block diagram of an apparatus for generating clock pulses using a DDS according to one embodiment of the present invention.

Best Mode for Carrying Out the Invention

[12] In the disclosure below, an embodiment of the present invention will be described in detail with reference to the accompanying drawing.

[13] Fig. 2 is a functional block diagram of an apparatus for generating clock pulses using a DDS 100 according to one embodiment of the present invention. Referring to Fig. 2, the apparatus comprises a DDS 100 including the following elements: a 10X PLL multiplier 101; a phase accumulator 102; a phase-to-magnitude converter 103; a Digital-to-Analog (DA) converter 104; a band pass filter 200; and a comparator 300.

[14] 10X PLL multiplier 101 within the DDS 100 receives 19.6608 MHz system reference clock pulses, converts the system reference clock pulses into 196.608 MHz DDS operation clock signals and provides the DDS operation clock signals to phase accumulator 102, phase-to-magnitude converter 103 and DA converter 104, respectively.

[15] Phase accumulator 102 within the DDS 100, which operates using the DDS operation clock signals from 10X PLL multiplier 101, receives a FTW in a binary format and accumulates a phase by the FTW to output the phase of a particular desired frequency to phase-to-magnitude converter 103.

[16] Phase-to-magnitude converter 103 within DDS 100, which operates using the DDS operation clock signals from the 10X PLL multiplier 101, receives the accumulated phase of the particular frequency from the phase accumulator 102, converts the phase value into a corresponding magnitude of a sinusoidal wave of the particular frequency, and outputs the sinusoidal signal to DA converter 104.

[17] DA converter 104 within DDS 100, which operates using the DDS operation clock signals from the 10X PLL multiplier 101, receives the sinusoidal signal from the phase-magnitude converter 103, converts the signal to an analog signal and output the analog signal of a DDS output frequency to band pass filter 200.

[18] The DDS output frequency can be derived from equation (1) below. The FTW, which is used to change the output frequency, can be derived from equation (2) below.

[19] $$f_{out} = (W * f_{clk})/2^N \quad (1)$$

[20] where f_{out} is an output frequency, W is a binary value for the FTW, f_{clk} is an operation clock frequency, and N is the number of input bits of phase accumulator 102.

[21] $$W = INT[(f_{out}/f_{clk})*2^N] \quad (2)$$

[22] where INT[] denotes an integer part of the bracketed expression.

[23] Band pass filter 200 receives the analog signal of the DDS output frequency from the DA converter 104. It then passes and outputs the signal only over a desired band of the DDS output frequency to comparator 300. In this case, band pass filter 200 may produce a clean sinusoidal waveform by removing unnecessary spurious signals, harmonics signals, etc. Further, a low pass filter may be used to pass only the

frequencies lower than a particular frequency.

[24] Comparator 300 receives the signal over the desired band of the DDS output frequency from band pass filter 200, transforms the signal of the DDS output frequency into a square wave with a low jitter, and outputs the square wave. Furthermore, comparator 300 has a precise zero-crossing threshold, and thus may output the square wave free from jitter and phase noise.

[25] There is provided a description of a procedure for generating clock pulses using the apparatus according to the present invention. Such apparatus comprises the DDS which is configured as noted above.

[26] First, 10X PLL multiplier 101 within DDS 100 receives 19.6608 MHz system reference clock pulses, converts the system reference clock pulses into 196.608 MHz DDS operation clock signals and output the DDS operation clock signals to phase accumulator 102, phase-to-magnitude converter 103 and DA converter 104, respectively.

[27] Subsequently, phase accumulator 102 operates using the DDS operation clock signals from 10X PLL multiplier 101 and receives a FTW in a binary format. It then accumulates a phase by the FTW to output the phase of a particular desired frequency to phase-to-magnitude converter 103.

[28] Then, phase-to-magnitude converter 103 operates using the DDS operation clock signals from the 10X PLL multiplier 101, receives the accumulated phase of the particular frequency from phase accumulator 102, converts the phase value into a corresponding magnitude of a sinusoidal wave of the particular frequency, and outputs the sinusoidal signal to DA converter 104.

[29] Thereafter, DA converter 104 operates using the DDS operation clock signals from the 10X PLL multiplier 101. It then receives the sinusoidal signal, which has the magnitude associated with the phase value of phase accumulator 102, from the phase-magnitude converter 103, converts the signal to an analog signal, and output the analog signal of a DDS output frequency to band pass filter 200.

[30] By way of an example, a method for deriving the output frequency of DDS 100 and the FTW is illustrated below.

[31] If it is assumed that the DDS operation clock frequency is 196.608 MHz, the output frequency is 58.9824 MHz and the number N of input bits of phase accumulator 102 is 48, then it becomes 59.9824 MHz = FTW * 196.608 MHz / 2^{48} when applying the above equation (1). Therefore, the FTW is (58.9824 MHz * 2^{48}) / 196.608 MHz. By equation (2), the FTW becomes 4CCCCCCCCCCD in hexadecimal, or 010011001100110011001100110011001100110011001101 in binary.

[32] Through the above calculation, the FTW can be obtained. By controlling the value of the FTW, it is possible to change the output frequency of DDS 100.

[33] Subsequently, band pass filter 200 receives the analog signal of the DDS output frequency from the DA converter 104, passes the signal only over a desired band of the DDS output frequency to comparator 300 to produce a dean sinusoidal waveform by removing unnecessary spurious signals, harmonics signals, etc. included in the DDS output frequency signal, and output the signal to comparator 300.

[34] Then, comparator 300 receives the signal over the desired band of the DDS output frequency from band pass filter 200, transforms the signal of the DDS output frequency into a square wave, where jitter and phase noise are removed by using a precise zero-crossing threshold.

[35] The above apparatus for generating dock pulses using DDS 100 can produce $2^{N}-1$ different frequencies signals ranging from 0 to half of the operation frequency with an increment of $1/2^{N}$, where N is the number of the input bits of phase accumulator 102.

Industrial Applicability

[36] As described above, according to the present invention, a particular desired frequency may be produced by changing the FTW when generating the dock pulses using the DDS. This is so that the output frequency can be changed more flexibly than the conventional dock generator using a PLL. Further, better stable system dock pulses can be supplied by removing jitter, phase noise, etc.

[37] While the present invention has been shown and described with respect to a preferred embodiment, those skilled in the art will recognize that various changes and modifications may be made without departing from the scope of the invention as defined in the appended daims.